

REMARKS

Claims 1, 3, 5-12, 14-15, 17-18, 20, 24-27, and 32-35 are pending in the application.

Claims 1, 3, 5-12, 14-15, 17-18, 20, 24-27 and 32-35 are rejected.

Claims 1, 6, 7, and 24-27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Deering (U.S. Pat. No. 5,544,306) in view of Shiraishi (U.S. Pat. No. 5,828,378).

Claims 3, 5, 8-12, 14, 15, 17, 18, and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Deering (U.S. Pat. No. 5,544,306) and Shiraishi (U.S. Pat. No. 5,828,378) in view of Dowdell (U.S. Pat. No. 5,301,263).

Claims 32-34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ryherd (U.S. Pat. No. 4,970,499).

Claim 35 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Ryherd (U.S. Pat. No. 4,970,499) in view of Dowdell (U.S. Pat. No. 5,301,263).

Claims 1, 10, 12, 18 and 32 have been amended.

Claim 17 has been cancelled.

No new subject matter has been added.

The Applicant respectfully requests reconsideration of claims 1, 3, 5-12, 14-15, 18, 20, 24-27, and 32-35.

Examiner Interview Summary

A telephonic Examiner Interview was conducted on March 3, 2008 between Mr. David Crowther, as representative of the Applicants, and Examiner Joni Hsu. Claims 1, 10, 17, 32, and 35 were discussed during the interview. A tentative agreement was reached that if independent claims 1 and 32 were amended to include limitations generally corresponding with claim 35, that claims 1 and 32 would likely be allowable. Examiner Hsu also indicated that the subject matter of claims 10 and 17 (a first status signal indicating that the lower X bits of the internal depth data have been modified, and a second status signal indicating that the upper X bits of the internal depth data have been modified) does not appear to be taught by the cited references, and likely would be allowable. The representative for the Applicants indicated to the Examiner that such amendments would need approval by the Applicants. Similarly, the Examiner indicated that the tentative agreement would need to be reviewed and agreed upon by the Examiner's supervisor.

In the Office Action dated January 22, 2008, the Examiner rejected claims 1, 6, 7, and 24-27 under 35 U.S.C. § 103(a) as being unpatentable over Deering (U.S. Pat. No. 5,544,306), hereinafter “Deering” in view of Shiraishi (U.S. Pat. No. 5,828,378), hereinafter “Shiraishi.” The Applicant respectfully traverses the rejection.

Claim 1 has been amended to set forth “the memory device comprising: a memory cell array adapted to store internal depth data of an object; a compare circuit; a line connecting the compare circuit to the memory cell array; and a data modifying circuit distinct from the memory controller, the data modifying circuit including the compare circuit and being adapted to: receive an activate command from the memory controller, receive corresponding new external depth data of the object from the memory controller, compare the new external depth data with the internal depth data, transfer the external depth data, via the connecting line, into the memory cell array, depending on the result of the comparison, if the external depth data is transferred, overwrite the internal depth data in the memory cell array with the transferred external depth data, and output to the memory controller a status signal within predetermined clock cycles from receipt of the activate command from the memory controller.” Claim 1 is amended to include limitations generally corresponding with the second element of claim 32 and claim 35. Specifically, claim 1 now includes the addition of the “receive an activate command from the memory controller,” which is similar to the second element of claim 32. Further, claim 1 now sets forth that the data modifying circuit is adapted to “output to the memory controller a status signal within predetermined clock cycles from receipt of the activate command from the memory controller.”

The Applicant submits that the amendment clarifies the scope of claim 1, and respectfully requests that the amendment be entered, and that claim 1 be allowed. To be sure, Deering, Shiraishi, and Ryherd fail to disclose that the data modifying circuit is adapted to receive an activate command from the memory controller, much less to output to the memory controller a status signal within a predetermined number of clock cycles from receipt of the activate command from the memory controller, as set forth in amended claim 1. Thus, amended claim 1 is patentable under 35 U.S.C. § 103(a) over the above references, as are dependent claims 6, 7, and 24-27.

In the Office Action dated January 22, 2008, the Examiner also rejected claims 3, 5, 8-12, 14, 15, 17, 18, and 20 under 35 U.S.C. § 103(a) as being unpatentable over Deering (U.S. Pat.

No. 5,544,306) and Shiraishi (U.S. Pat. No. 5,828,378) in view of Dowdell (U.S. Pat. No. 5,301,263), hereinafter “Dowdell.” The Applicant respectfully traverses the rejection.

Based at least on their dependency from amended claim 1, and for their own merits, claims 3, 5, 8-9, and 11 are allowable.

Claim 10 has been amended to include the limitations of claim 1. Based at least on the Examiner’s indication during the interview (summarized above) that the limitations of claim 10 (a first status signal indicating that the lower X bits of the internal depth data have been modified, and a second status signal indicating that the upper X bits of the internal depth data have been modified) do not appear to be taught by the cited references and would likely be allowable, the Applicant submits that claim 10 is now in proper form for allowance.

The Examiner suggested in the Office Action dated January 22, 2008 that this is taught at column 4, lines 3-10 of Dowdell (Office Action, page 9). However, Dowdell teaches that “[f]or a given z-buffer address . . . the INVALID bit for a particular pixel indicates whether or not the corresponding z-value memory location has a valid z-value stored in it, with a value of ‘0’ indicating that it does and a value of ‘1’ indicating that it does not” (Dowdell, column 4, lines 3-10). In contrast, Dowdell fails to disclose “a first status signal indicating that the lower X bits of the internal depth data have been modified, and a second status signal indicating that the upper X bits of the internal depth data have been modified” as set forth in claim 10. Deering and Shiraishi fail to remedy the defects of Dowdell. Thus, claim 10 is patentable under 35 U.S.C. § 103(a) over Deering and Shiraishi even when viewed with Dowdell.

Claim 12 has been amended to include the limitations of claim 17, which has been cancelled. For substantially the reasons set forth above with respect to claim 10, claim 12 is patentable under 35 U.S.C. § 103(a) over Deering and Shiraishi even when viewed with Dowdell, as are dependent claims 14, 15, 18, and 20. Claim 18 has been amended to depend from claim 12 rather than claim 17.

Claims 32-34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ryherd (U.S. Pat. No. 4,970,499), hereinafter “Ryherd.”

Claim 35 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Ryherd (U.S. Pat. No. 4,970,499) in view of Dowdell (U.S. Pat. No. 5,301,263).

The Applicant respectfully traverses the rejections.

Claim 32 has been amended to set forth a method for processing depth data of an object in a memory device controlled by a memory controller, the method comprising: “generating at

least seven clock cycles; receiving an activate command from the memory controller responsive to a first of the at least seven clock cycles; receiving a depth-compare write command from the memory controller responsive to a third of the at least seven clock cycles; receiving external depth data responsive to the third of the at least seven clock cycles, the external depth data indicating a distance between the object on a display screen and a viewer; receiving at least one control signal from the memory controller responsive to the third of the at least seven clock cycles; comparing the received external depth data with internal depth data stored in a memory cell array of the memory device, the comparing being completed before one of a sixth and a seventh of the seven clock cycles, wherein at least one status signal is transmitted from the memory device to the memory controller, the at least one status signal indicating whether the internal depth data was replaced with the external depth data, the at least one status signal being transmitted responsive to a predetermined number of clock cycles.”

Specifically, the limitation of “wherein at least one status signal is transmitted from the memory device to the memory controller, the at least one status signal indicating whether the internal depth data was replaced with the external depth data, the at least one status signal being transmitted responsive to a predetermined number of clock cycles” has been added to claim 32. Dowdell and Ryherd fail to disclose the at least one status signal being transmitted responsive to a predetermined number of clock cycles. Nowhere does Dowdell nor Ryherd teach this, whether individually or in combination with each other. Thus, claim 32, as amended, is patentable under 35 U.S.C. § 103(a) over Ryherd and Dowdell, as are dependent claims 33 and 34.

Claim 35 sets forth the method of claim 34, “wherein at least one status signal is transmitted from the memory device to the memory controller, the at least one status signal indicating whether the internal depth data was replaced with the external depth data, the at least one status signal being transmitted responsive to one of the sixth and the seventh of the seven clock cycles.” Deering, Shiraishi, and Ryherd fail to disclose at least one status signal is transmitted from the memory device to the memory controller, much less the at least one status signal being transmitted responsive to one of the sixth and the seventh of the seven clock cycles, as set forth in claim 35. Thus, claim 35 is patentable under 35 U.S.C. § 103(a) over Ryherd and Dowdell.

For the foregoing reasons, reconsideration and allowance of claims 1, 3, 5-12, 14-15, 18, 20, 24-27, and 32-35 of the application as amended is requested. The Examiner is encouraged to

telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



Alan T. McCollom
Reg. No. 28,881

MARGER JOHNSON & McCOLLOM, P.C.
210 SW Morrison Street, Suite 400
Portland, OR 97204
503-222-3613

Customer No. 20575